

FIG. 1

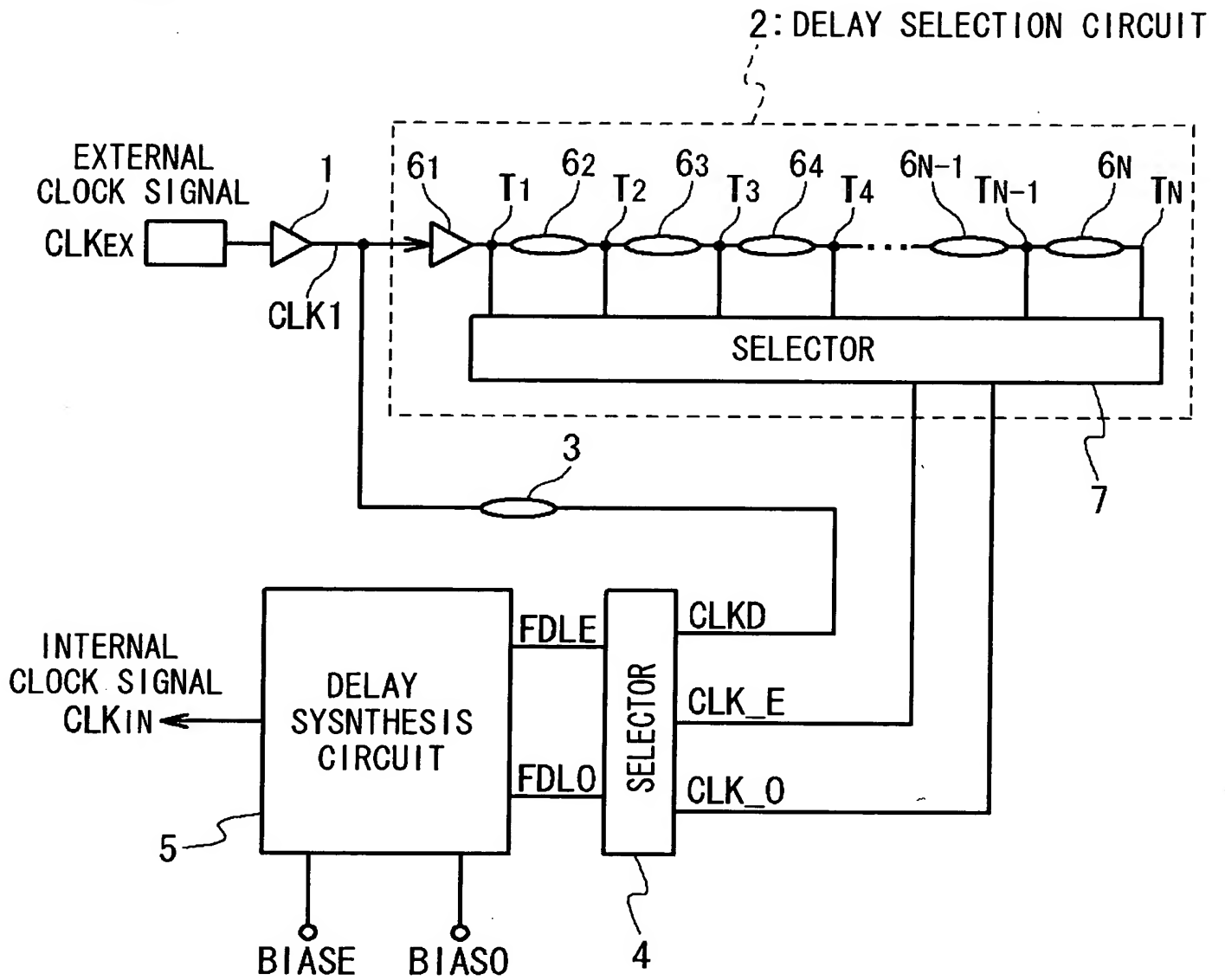


FIG . 2

5: DELAY SYNTHESIS CIRCUIT

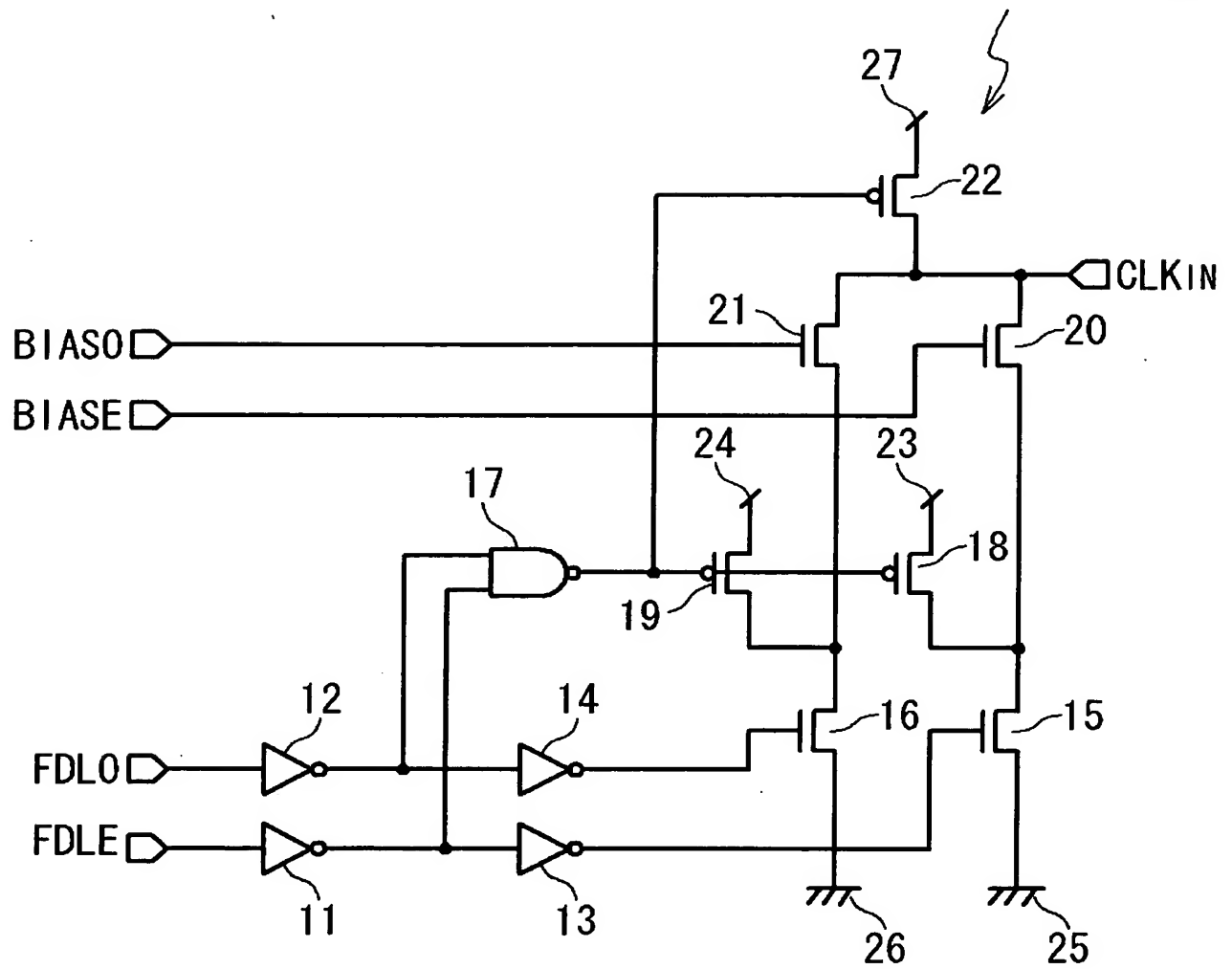


FIG . 3

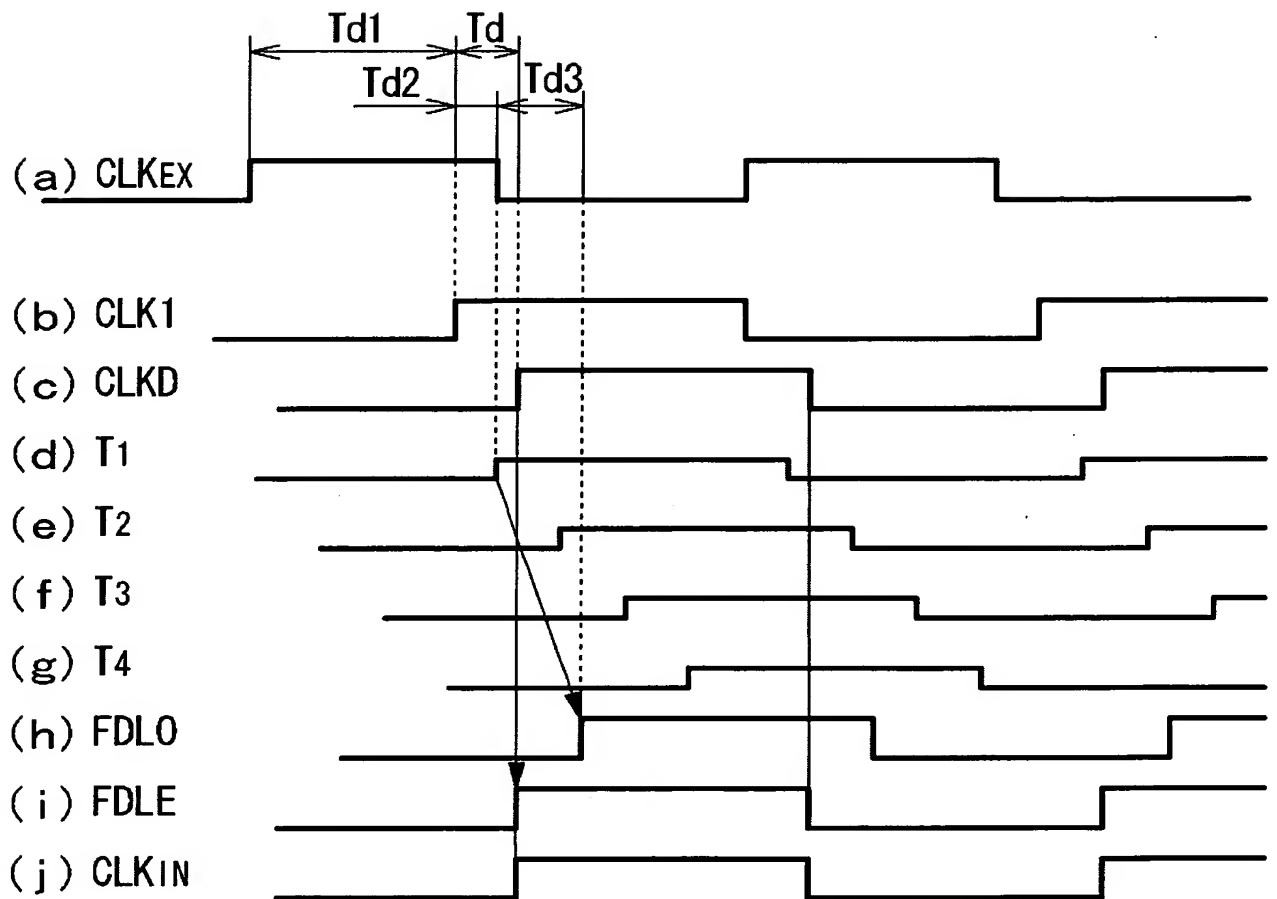


FIG . 4

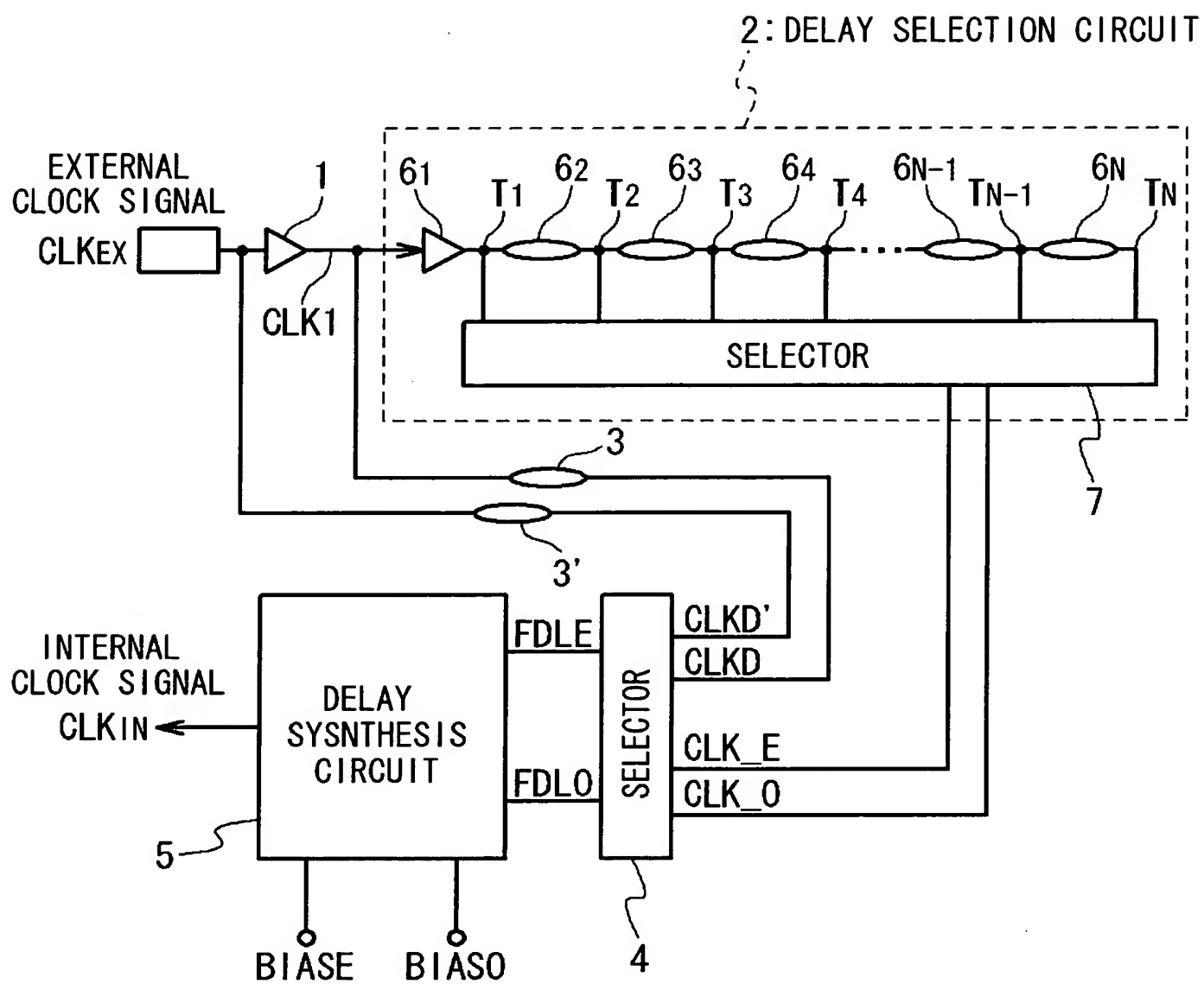


FIG . 5

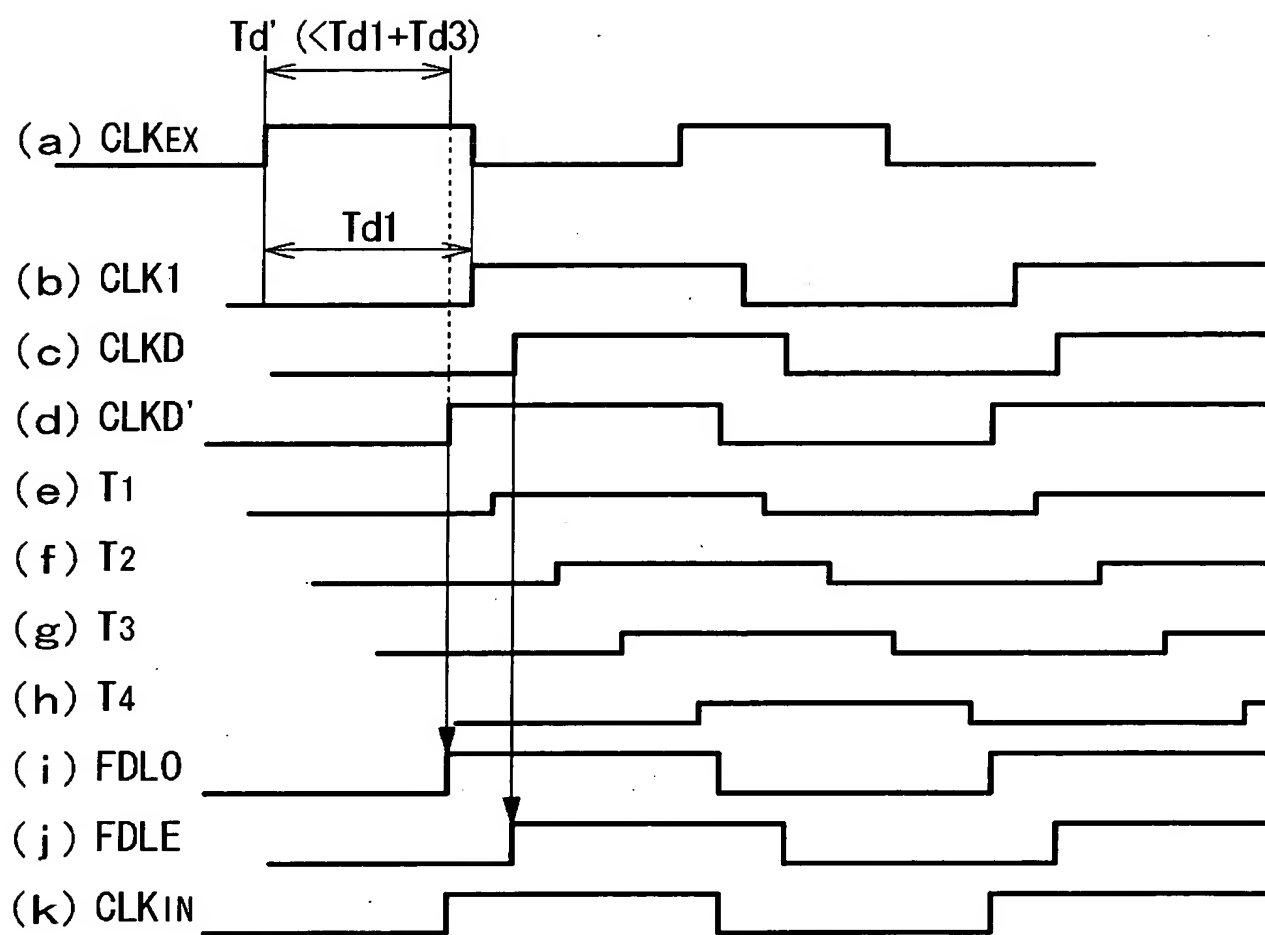


FIG . 6

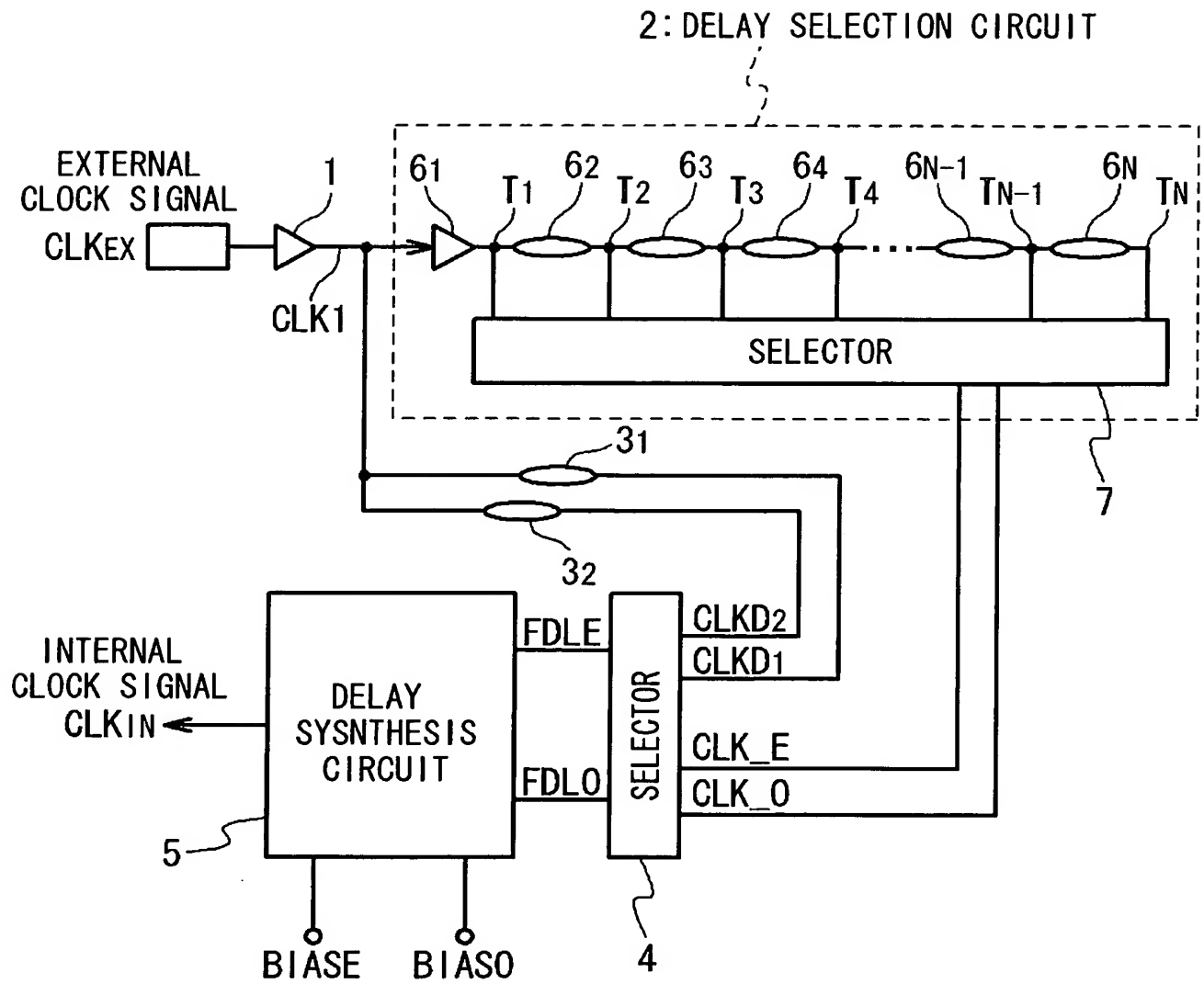


FIG . 7

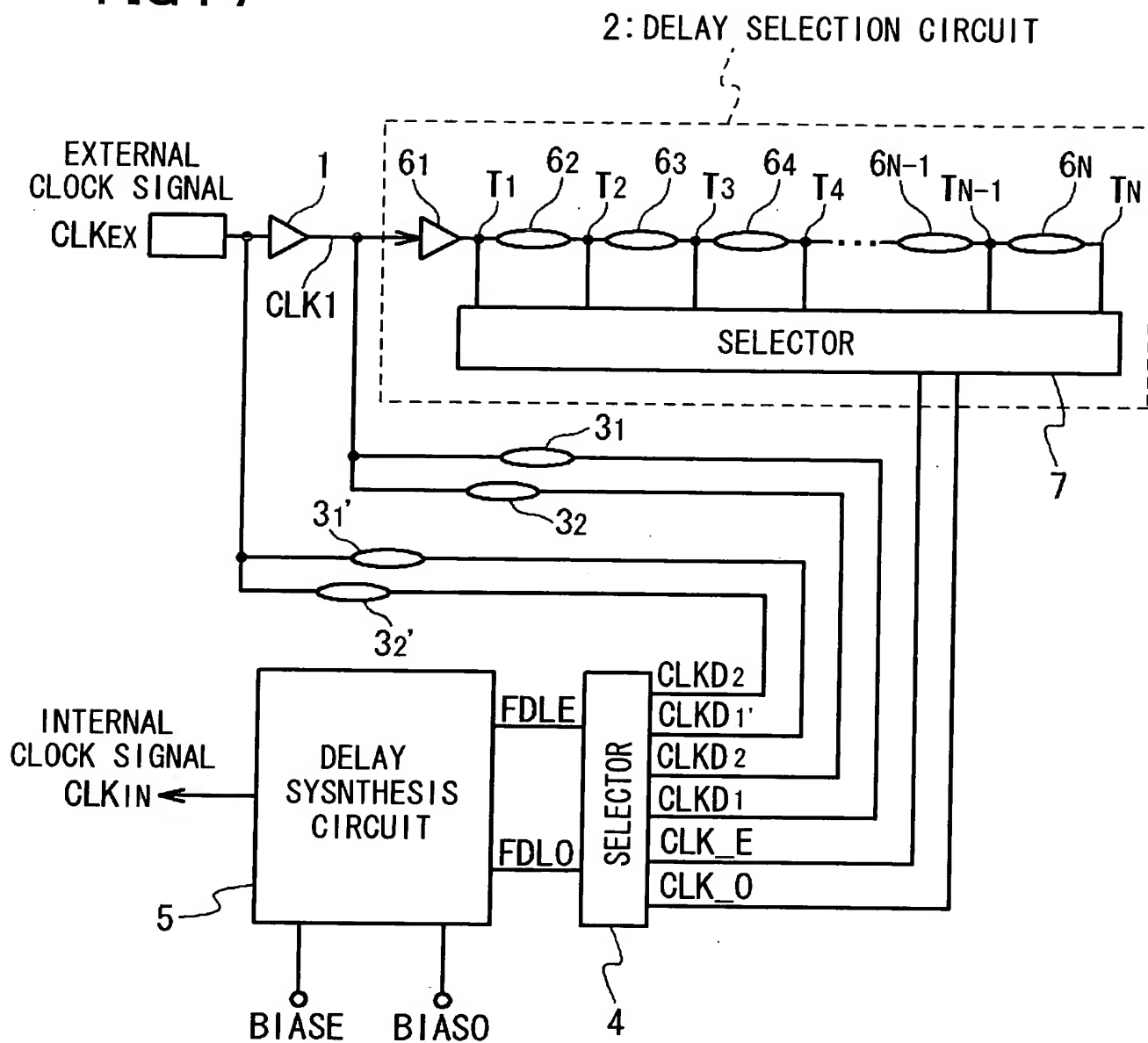


FIG . 8 PRIOR ART

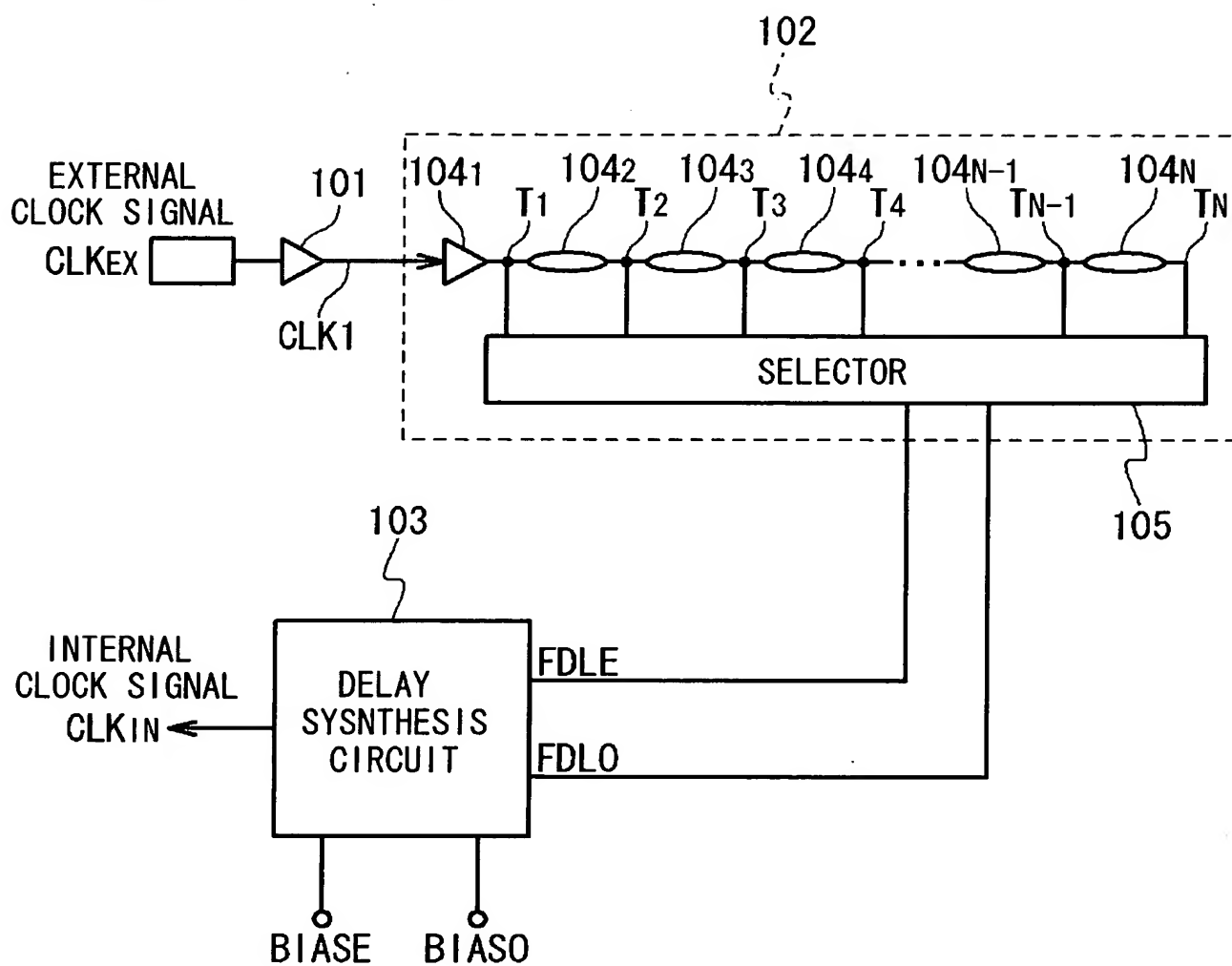




FIG . 9 PRIOR ART

